REMARKS

At the time of the Office Action dated July 19, 2004, claims 1-20 were pending. Applicants acknowledge, with appreciation, the Examiner's allowance of claims 17-20.

Claims 1-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lepejian et al. in view of Adams et al.

In the statement of the rejection, the Examiner admitted that Lepejian et al. does not teach a BIST circuit comprising a programmable algorithmic pattern generator. The Examiner then cited Adams et al., asserting that the reference teaches a BIST circuit that tests a multi-port array in concert with a programmable pattern generator that allows different R/W data operations to be performed at the same or adjacent address locations. The conclusion was that it would have been obvious to modify Lepejian's BIST circuit to include a programmable pattern generator as taught by Adams et al. This rejection is respectfully traversed.

Applicants submit that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Based on the above legal tenet, Applicants specifically submit that the proposed combination of Lepejian et al. and Adams et al. does not teach or suggest a semiconductor memory device including a built-in self test circuit comprising "a programmable Algorithmic Pattern Generator (ALPG) to generate said address signal according to said stored program and generate said test data according to said generated address signal," as recited in claim 1 (emphasis added). In other words, the proposed combination does not teach the ALPG

configured for generating the test data based on the address signal. Since as the Examiner admitted, Lepejian et al. does not teach the ALPG, Applicants will discuss whether Adams et al. teaches the ALPG below.

The claimed invention employs a microinstruction scheme in which a pattern (e.g., command, address, data) is generated in accordance with program contents in a loaded instruction memory. On the other hand, Adams et al. employs an operation of several sequences in accordance with a value set in a predetermined data latch.

Furthermore, test data generation in the claimed invention is different from that of Adams et al. In the claimed invention, the test data is generated based on the address. In contrast, data is generated in accordance with the data latch set by scanning through a data generator.

In testing a memory array, it is important to generate a data pattern taking into consideration physical information of that memory array. Accordingly, the claimed invention includes address information for data generation. For example, a data pattern such as a cell checker pattern taking into consideration the physical information of the memory array can be generated in the claimed invention. However, it is not possible for Adams' circuit to do that. In other words, Adams' testing of the memory array is insufficient.

Therefore, it is apparent that the ALPG of the claimed invention is different from Adams' pattern generator. Specifically, Adams et al. does not teach the ALPG configured for generating the test data based on the address signal.

Thus, the proposed combination of Lepejian et al. and Adams et al. does not teach or suggest a semiconductor memory device including all the limitations recited in claim 1. In the instant case, the pending rejection has not established *prima facie* obviousness of the claimed

invention as recited in claim 1, because the proposed combination fails to teach all the claim limitations, as required under §103. *See In re Royka*, 490 F.2d 981.

It is noted that if an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Accordingly, as claim 1 is patentable for the reasons set forth above, it is submitted that dependent claims 2-16 which respectively depend from claim 1 are also patentable. The Examiner's additional comments with respect to the claims do not cure the argued fundamental deficiencies of the proposed combination of Lepejian et al. and Adams et al.

Applicants, therefore, respectfully solicit withdrawal of the rejection of claims 1-16 under 35 U.S.C. §103(a) and favorable consideration thereof.

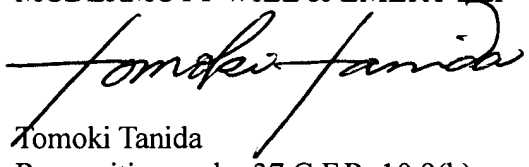
Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



Tomoki Tanida
Recognition under 37 C.F.R. 10.9(b)

600 13th Street, N.W.
Washington, DC 20005-3096
202.756.8000 SAB:TT
Facsimile: 202.756.8087
Date: October 19, 2004

WDC99 991993-1.049657.0875

BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
UNITED STATES PATENT AND TRADEMARK OFFICE

LIMITED RECOGNITION UNDER 37 CFR § 10.9(b)

Mr. Tomoki Tanida is hereby given limited recognition under 37 CFR §10.9(b) as an employee of McDermott, Will & Emery to prepare and prosecute patent applications in which the patent applicant is the client of McDermott, Will & Emery and the attorney or agent of record in the applications is a registered practitioner who is a member of McDermott, Will & Emery. This limited recognition shall expire on the date appearing below, or when whichever of the following events first occurs prior to the date appearing below: (i) Mr. Tomoki Tanida ceases to lawfully reside in the United States, (ii) Mr. Tomoki Tanida's employment with McDermott, Will & Emery ceases or is terminated, or (iii) Mr. Tomoki Tanida ceases to remain or reside in the United States on an H-1B visa.

This document constitutes proof of such recognition. The original of this document is on file in the Office of Enrollment and Discipline of the U.S. Patent and Trademark Office.

Expires: June 1, 2006

Harry I. Moatz
Director of Enrollment and Discipline